REMARKS

The Examiner's Final Action mailed on July 9, 2003 has been received and its contents have been carefully considered.

Claims 1-15 are pending in this application. In this Amendment, Applicants have amended claims 1 and 9, the independent claims, to define the invention more particularly and distinctly. For at least the following reasons, it is submitted that this application is in condition for allowance.

In the Final Office Action, claims 1-15 are first rejected under 35 U.S.C. 102(b) as anticipated by the Applicants' Admitted Prior Art (AAPA). The rejection is respectfully traversed.

The Examiner's rejection of the pending claims as anticipated by the AAPA was not previously asserted and is new. Before addressing the rejection on its merits, it is noted that this basis for rejection is asserted in the Action in a single sentence without any supporting argument or rationale. Thus, the Examiner has completely failed meet the requirements of MPEP 706.07, namely, to clearly develop in the record the grounds relied on in the final rejection. For this reason alone, it is respectfully requested that the finality of the rejection be withdrawn.

As to the merits of the rejection, as best understood, it is respectfully submitted that the AAPA fails to disclose in any way a "second pad for probing ... formed on an IC" or a "plurality of second pads arranged ... on the IC," as recited in the claims. In describing the prior art, the application (page two lines 15-21) states only:

> While the step of the IC function and reliability testing 103 is performed, the probes need to be inserted to connect the bonding pad for testing the IC. As shown a Figure 2, however, it is used to cause probing damage and make the bonding pad rough and uneven in surface after probing (as indicated by arrow 301). Sometimes the probes may punch holes in the metal surface layer of the bonding pad. The damaged bonding pad is harmful for the step of wire bonding and packaging 104 and decreases the yield rate of IC products.

Thus, the AAPA teaches that the probes for testing are applied to the pads intended for bonding, and not, as in the present invention, to separate pads, electrically connected to the bonding pads, that are distinctly intended for probing.

In the current Action, claims 1-15 are also rejected on the grounds set forth in the previous Office Action, dated March 18, 2003. Specifically, claims 1-3 (and presumably corresponding claims 9-11) stand rejected under 35 U.S.C. §102(b) as being anticipated by Nakamura (US Patent No. 5,982,042), and claims 4-8 (and presumably corresponding claims 12-15) stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura in view of Kudou et al. (US Patent No. 6,303,948). It is respectfully submitted that these claims, as presently amended, patentably distinguish over the cited references for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 U.S.C. §102 only if all the features and all the relationships recited in the claim are taught by the reference either by clear disclosure or under the principle of inherency. However, the cited reference does not disclose, nor does it even suggest, all of the features recited in amended independent claim 1.

Applicants' amended claim 1 recites a bonding pad structure comprising: a first pad for bonding; and at least one second pad for probing, coupled with the first pad, wherein both of the first pad and the second pad are formed on an IC (Integrated Circuit) and remain in whole as part of the IC after fabrication (emphasis added).

In responding to the arguments made by the Applicants in the Amendment submitted June 18, 2003, the Examiner points to Nakamura as disclosing that a wire-bonding pad 2 and a testing pad 3 are formed on the integrated circuit formation regions on the semiconductor wafer 1 (column 4, lines 44-53 and Figure 8). The text in column 4 referenced by the Examiner actually refers to Figures 1-7, which disclose a first embodiment in which a small portion 3a of the probe pad is formed on the semiconductor integrated circuit formation region, and hence, remains on each finished chip after dicing (see column 5, lines 10-13 and Figure 7). However, the added language in amended claim 1, "and remain in whole as part of the IC after fabrication," clearly distinguishes over Nakamura.

Figure 8 of Nakamura discloses a different embodiment that has a semiconductor wafer including a semiconductor device, wherein the semiconductor device has a wire-bonding pad 2, formed on the IC 1a; a wafer testing pad, formed on the dicing line 6, which is a cutting region around the IC 1a; and an extension aluminum interconnection 7 that electrically connects the wire-bonding pad 2 and the wafer testing pad 3 (Col. 6, line 8–12). Nakamura fails to disclose

(or suggest) that both of the first pad and the second pad are formed on the IC; instead, the wafer testing pad revealed by Nakamura is formed on the dicing line 6, which is a cutting region around the IC 1a, and removed after wafer testing. As such, it is submitted that this embodiment also fails to anticipate to the claimed invention because it lacks any disclosure that both the first and second pads "remain in whole as part of the IC after fabrication."

In the Action (page 3) the Examiner asserts that the semiconductor wafer could be an IC or a PCB. Neither the application nor the Nakamura reference support such an expansive reading of the terms used in the claims. Nakamura clearly discloses that after wafer testing is finished, the wafer is cut along dicing lines so that the semiconductor integrated circuits (i.e., IC's) are separated into chips (column 1, lines 19-22). Similarly, Figure 1 of the application shows wafer fabrication followed by testing of the individual IC's. Thus the terms IC and PCB refer to individual chips or boards, and this is emphasized in the amended claims by the phrase "after fabrication".

With regard to claims 2 and 3, it is submitted that they patentably distinguish over the cited reference for at least the same reasons that independent claim 1 is allowable, since claims 2 and 3 depend from claim 1. It therefore is submitted that the rejection is overcome by the amended claims, and accordingly, should be withdrawn.

With regard to claims 4-8, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first pad layout and the second pad layout arranged in a linear or staggered manner, as taught by Kudou et al.

Kudou et al. discloses a layout for pads and leads for a semiconductor device in order to cope with reductions in chip size, increases in the number of pins of a package, and reductions in the pitch of the pads. Kudou et al. lacks any teaching or suggestion regarding test pads or the arrangement of test pads on an IC. Accordingly, it is submitted that those skilled in the art would not be motivated to arrange the layouts for pads and leads, as taught by Kudou et al. in the device of Nakamura, except in a hindsight attempt at reconstructing Applicants' claimed invention, or to otherwise simply combine the teachings of the two references in the manner suggested by the Examiner to overcome the deficiency of Nakamura. For at least these reasons, the rejection is respectfully traversed.

In addition, it is submitted that claims 4-8 patentably distinguish over the applied references for at least the same reasons as independent claim 1, from which these claims depend. Therefore, it is respectfully requested that the rejection of claims 4-8 be withdrawn.

Applicants' independent claim 9 recites a bonding pad structure comprising: a first pad for bonding; and at least one second pad for probing, coupled with the first pad, wherein both of the first pad and the second pad are formed on a PCB (printed circuit board) and remain in whole as part of the PCB after fabrication. It is submitted that claim 9-15, as amended, patentably distinguish the invention over the cited references for essentially the same reasons as discussed above in connection with claims 1-8. Furthermore, neither Nakamura nor Kudou et al. teaches or suggests a bonding pad structure in which both of the first pad and the second pad are formed on a PCB (printed circuit board), as distinct from an IC. As such, it is submitted that claim 9 has not been anticipated by (or otherwise rendered obvious by) Nakamura and patentably distinguishes over the cited art combination, Nakamura in view of Kudou.

Based on the foregoing, it is submitted that all of the pending claims 1-15 are allowable over the cited references, so that this application is in condition for allowance. Accordingly, notice of allowance and the passing of this case to issue are respectfully requested.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

October 31, 2003
Date

Phillip G. Avruch
Registration No. 46,076
RABIN & BERDO, PC
Customer No. 23995
(202) 371-8976 (Telephone)
(202) 408-0924 (Facsimile)
firm@rabinchamp.com (E-mail)